

**REMARKS/ARGUMENTS**

Reconsideration of this application is requested. The independent claims have been amended in order to more particularly point out and distinctly claim that which applicants regard as their invention. No new matter is introduced. In the specification, clerical errors  
5 have been corrected in this amendment.

1. Corrections on Fig.2 and Fig.5:

The drawings were objected to because element 37 mentioned in the description is not included in the drawings. In reply to this, two replacement sheets have been respectfully resubmitted, wherein in figure 5, the wrong reference signs 38 and 39 have  
10 been replaced with the reference signs 36 and 37, respectively. Reconsideration of newly submitted Fig.5 is politely requested.

The Examiner further indicated that Fig.2 and Fig.4 disagree each other because Fig.2 discloses a tunneling connection between an extended  $N^+$  gate section 36 over a P-type electrically isolated body 15 in a P-type silicon thin film 16, while Fig.4 discloses  
15 the same tunneling connection wherein the extended  $N^+$  gate section 36 is now over a N-type extended body region 52.

For purposes of clarity, the reference numeral 52 has been added into Fig.2. However, applicants never teach that the electrically isolated body 15 is purely P type. In fact, as described in paragraph [0026], the electrically isolated body 15 is initially defined  
20 by STI regions and is fabricated within the N well 13. Therefore, the electrically isolated body 15 is N type before the source/drain 42 and 44 implant. As described in paragraph [0028] and also can be seen in figure 1, after the source/drain implant, the electrically isolated body 15 now includes channel region (N type) under the  $P^+$  gate 35, P type source/drain 42 and 44, and extended N type body region 52. It is respectfully noted that  
25 since figure 2 is depicted along line A-A of figure 1, the P type source/drain 42 and 44 is not shown in figure 2. Withdrawal of the objections to figures 2 and 4 is politely

requested.

2. Rejection of claim 1 under 102(e):

Claims 1, 3, 4 and 6 were rejected under 35 U.S.C. 102(e) for reason of record that  
5 can be found on pages 4-5 in the Office action identified above, which is Part of Paper  
No./Mail Date 20040827.

To overcome this 102 rejection, claim 1 has been amended. Ebina ('948) teaches a  
SOI field effect transistor including a gate electrode 24 that is in electrical contact with a  
P<sup>-</sup> region 16 via contact 34. The purpose of the SOI FET structure taught by Ebina ('948)  
10 is to provide a polysilicon PN junction diode, such that when in operation, only a small  
current of the PN junction flows through the gate electrode 24. The SOI FET structure  
taught by Ebina is not capable of forming a tunneling connection between the gate  
electrode 24 and the P<sup>-</sup> region 16. Ebina teaches away from that "a first gate section of  
first conductivity type overlapping and capacitively coupling with an extended well  
15 region", as required by the amended claim 1. Further, Ebina does not teach the limitation  
that "said polysilicon gate is not electrically connected to said well or said extended well  
region", as required by the amended claim 1. Reconsideration of the amended claim 1 is  
accordingly requested. As Claims 2-6 are dependent upon claim 1, they should be  
allowable if claim 1 is allowed. Reconsideration of claims 2-6 is politely requested.

20 3. Rejection of claim 7 under 103(a) and 112:

Claims 7-12 were rejected under 35 U.S.C. 103(a) for reason of record that can be  
found on pages 6-9 in the Office action identified above, which is Part of Paper No./Mail  
Date 20040827.

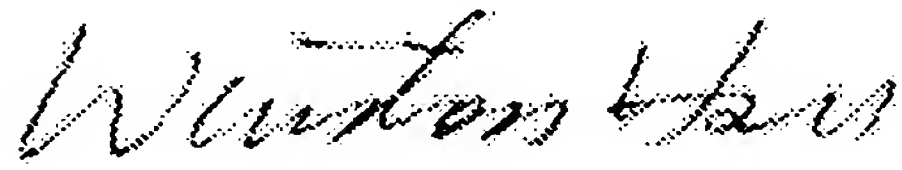
To overcome the 103 and 112 rejections, claim 7 has been amended. Applicants  
25 believe that the cited prior art references fail to teach that "said polysilicon gate is not  
electrically connected to said well" and the limitation "during operation, a channel

Appl. No. 10/605,481  
Amdt. Dated November 10, 2004  
Reply to Office action of September 08, 2004

electrical field near said drain region is reduced", as required by the amended claim 7. Ebina teaches a SOI field effect transistor including a gate electrode 24 that is in electrical contact with a P<sup>-</sup> region 16 via contact 34. Reconsideration of the amended claim 7 is  
5 accordingly requested. As Claims 8-12 are dependent upon claim 7, they should be allowable if claim 7 is allowed. Reconsideration of claims 8-12 is requested.

Applicants respectfully request that a timely Notice of Allowance be issued in this case.

10 Sincerely yours,



Date: NOV 11 2004

15 Winston Hsu, Patent Agent No. 41,526

P.O. BOX 506

Merrifield, VA 22116

U.S.A.

Voice Mail: 302-729-1562

20 Facsimile: 806-498-6673

e-mail : winstonhsu@naipo.com

(Please contact me by voice mail if you need a telephone communication.)

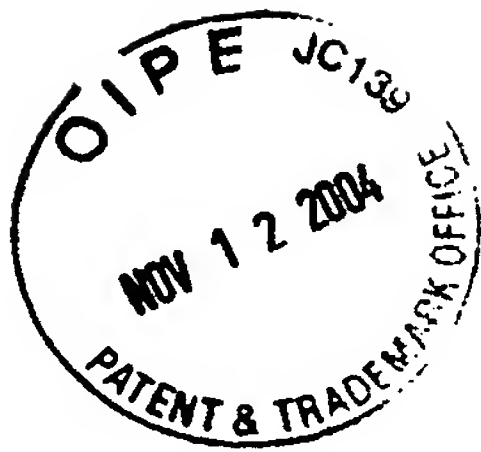
Attachment

Appl. No. 10/605,481  
Amdt. Dated November 10, 2004  
Reply to Office action of September 08, 2004

**Amendments to the Drawings:**

The attached two replacement sheets containing figure 2 and figure 5, respectively, replace the original two sheets of figures 2 and 5. No new matter is introduced.

- 5    Attachment:    Two Replacement Sheets  
                         Two Annotated Sheet Showing Changes



Annotated Sheet Showing Changes

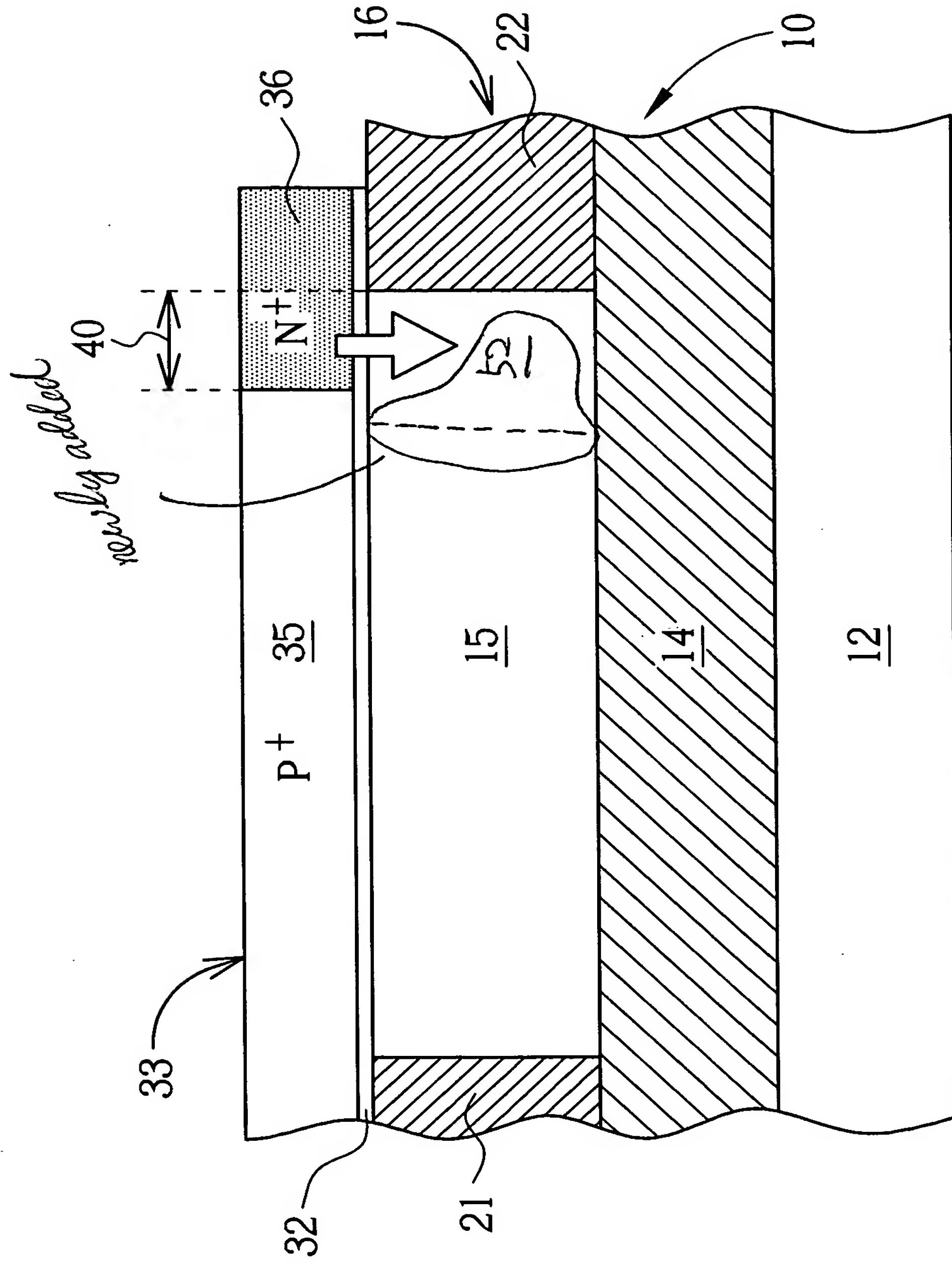


Fig. 2

